REMARKS

Reconsideration and withdrawal of the rejections set forth in the Office Action dated March 24, 2004 are respectfully requested. In that Office Action, Claims 1, 13-15 stand rejected under 35 USC 102 (e) as being as being anticipated by Bae et al. U. S. 2003/0094662. Claims 1-3, 13-21, 25-27 and 37-48 stand rejected under 35 USC 103 (a) as being unpatentable over Wu et al. (U. S. Patent No. 6,482,691) in view of Tsai et al (U.S. Patent No. 6,613,623). Claims 1, 5, 9, and 33 stand rejected under 35 USC 103 (a) as being un-patentable over Iguchi et al. (U. S. Patent No. 5,734,185) in view of Tsai et al. Claim 1 stands rejected under 35 USC 103 (a) as being un-patentable over Ryu (U.S. Patent No. 2002/0142523 A1) in view of Tsai et al. Claim 1 stands rejected under 35 USC 103 (a) as being un-patentable over Chatterjee et al. (U.S. Patent No. 6,180,978 B1) in view of Tsai et al.

The Examiner also indicated that Claims 4, 6-8, 10-12, 22-24, 28, 30-36 and 49-52 would be allowable if rewritten in independent form. Applicant has added new claims 53-75 which are the above mentioned claims rewritten in independent form. Claims 4, 6-8, 10-12, 22-24, 28, 30-36 and 49-52 have been cancelled. Applicant believes that all of the added new claims will be allowed.

Turning now to the rejection of the claims based upon the prior art, as known in the art of non-volatile memory (NVM), the memory cell requires hot carriers (electrons or holes) for charge injection into a trapping structure. Typically, the injection process takes place between the trapping structure and the source/drain (S/D) junction. For example, in U.S. Patent No. 6,545,309, at col. 1:

> The charge-trapping layer usually comprises a silicon nitride layer that is disposed between two silicon oxide layers to form an oxide/nitride/oxide (ONO) composite layer, while the memory with a nitride charge-trapping layer is known as a "nitride read-only memory (NROM)". In a NROM, the nitride charge-trapping is able to trap electrons so that the injected hot electrons will not distribute evenly in the charge-trapping layer, but will be localized in a region of the charge-trapping layer near the drain with a Gaussian spatial distribution. Because the injected electrons are localized, the charge-trapping region is small and is less likely to locate on the defects of the tunnel oxide layer. A leakage therefore does not easily occur in the device.

U.S. Patent No. 6,618,286 states:

> FIG. 10A illustrates normal write operation of MONOS memory transistor cell... When 0 V is applied to P-type semiconductor substrate 1, 10 V is applied to control gate 7, 5 V is applied to diffusion region 2, and 0 V is applied to diffusion region 3, channel electrons are accelerated by a steep electric field created in diffusion region 2 of the memory transistor cell. Those accelerated electrons which overcome the barrier height of the oxide film are trapped on the side of diffusion region 2 in nitride film 5 (bit 1)...

In contrast, the specification of the present application recites at page 30: **"The hot electrons or holes are trapped as they are injected into the Spacer 12 via the injection portion near the S/D junction 10 over the substrate 2."** The part of the isolation layer over the substrate under the trapping structure is used as a potential barrier to retain charges. It can be seen in all of the Figures of the application that the injection portion is formed between the trapping structure and the S/D junction.

1. Rejection under 35 USC 102 (e) as being as being anticipated by Bae et al.

Bae discloses a MOS transistor having a T-shaped gate electrode. In the Office Action, the Examiner argues that Bae discloses a gate structure having an undercut structure. Applicant would like to emphasize that the citation of Bae is a MOS transistor that is used as a switch. The present claimed invention is a NVM (nonvolatile memory). Thus, the Bae patent is not analogous art. NVM requires charge injection aligned with a charge trapping layer (or structure) to store carriers or charge, whereas MOS is a switch which does not require "injecting and storing carriers" as claimed. In normal MOS transistor operation mode, the spacer is used as isolation for the gate and to form LDD structure instead of storing charge. Thus, Bae does not anticipate the application under 35 USC 102 (e) since Bae fails to teach a storing charge undercut structure for NVM. In fact, the Bae transistor structure will fail if the undercut (part of spacer) stores charge. Bae fails to disclose the injection portion.

Further, in Bae, the material that forms the undercut is a lower insulating layer 170 (spacer). The spacer in a MOSFET is used to create a doped region instead of forming a trapping structure. Therefore, there is no motivation for Bae to form an undercut structure for trapping or storing carriers. In the claims, the undercut portion has a specific function to trap charges which are from an aligned injection structure for nonvolatile memory.

2. Rejection of Claims 1-3, 13-21, 25-27 and 37-48 under 35 USC 103 (a) as being un-patentable over Wu et al. in view of Tsai et al.

Similarly, Wu discloses a field effect transistor instead of NVM or nonvolatile memory. Thus, Wu is not analogous art. NVM needs a charge trapping structure with an aligned injection structure to inject and store carriers or charge. MOSFETs do not perform such a function, and therefore, no structure "for storing carriers" is needed. Thus, the same arguments above with respect to Bae apply equally to Wu.

The Examiner further argues that Wu does not disclose a silicide, and for this teaching relies upon Tsai. However, there is not any suggestion or motivation for such a combination.

3. Rejection of Claims 1, 5, 9, and 33 under 35 USC 103 (a) as being un-patentable over Iguchi et al. (U. S. Patent No. 5734185) in view of Tsai et al (U.S. Patent No. 6613623).

Iguchi also discloses a MOS transistor and fabrication process therefore. Once again, this is not nonvolatile memory. Thus, the prior art leads to an entirely different field and is not analogous art. For the same reasons stated above, Iguchi does not render obvious the claimed invention since Iguchi does not teach a structure "for storing carriers". Iguchi simply fails to teach the storing charge undercut structure for NVM.

4. Rejection Claim 1 under 35 USC 103 (a) as being un-patentable over Ryu in view of Tsai et al.

Ryu provides a semiconductor device that reduces gate capacitance according to the reduction of gate length by forming a notched gate. Thus, Ryu's notched structure is for reducing gate length instead of charge trapping. Ryu states that the semiconductor device is used for forming a transistor and therefore is not analogous art. NVM requires a charge trapping structure to store carriers or charges; no injection portion and structure "for storing carriers" are needed in MOS. More important, Ryu fails to disclose the injection portion and undercut charge trapping structure as cited in the claims.

5. Rejection of Claim 1, 5, 25 and 29 under 35 USC 103 (a) as being un-patentable over Chatterjee et al. (U.S. Patent No. 6180978 B1) in view of Tsai et al (U.S. Patent No. 6613623).

Chatterjee teaches a disposable gate/replacement gate MOSFETs and again is in non-analogous art. No structure "for storing carriers" are needed in a MOSFET. Similarly, Chatterjee fails to disclose the undercut charge trapping structure and injection portion as cited in the claims.

In view of the foregoing, the claims pending in the application comply with the requirements of 35 U.S.C. § 112 and patentably define over the applied art. A Notice of Allowance is, therefore, respectfully requested. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-8000.

Respectfully submitted,

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